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(54) MEMORY DEVICE

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a memory device.

MNOS devices, which are formed from layers of metal, silicon nitride and silicon dioxide on the surface of a semiconductor substrate, are well known. In such devices, charge is stored at unknown trapping centres at the nitride-oxide interface. The oxide is very thin (approximately 30—50Å) and a mechanism for populating the interface states is by tunneling from the adjacent semiconductor substrate. Storage of charge at the interface of two insulators can be achieved using most of the known insulators but the reproducibility magnitude of the effect, particularly at room temperature, is limited. Recent publications have suggested the use of a metallic layer between two insulating films of appropriate characteristics for the storage of charge carriers in the metallic layer. The same literature also suggests the use of a discontinuous metal layer to minimize the effect of pinholes in an underlying insulating layer. This discontinuous layer, however, is conductive in the sense that current can flow through the film from one side to the other indicating an electrical conductivity or interacting relationship between different portions of the discontinuous film. In such devices the charge which tunnels is stored on a discontinuous conductive film.

Other recent literature shows devices called tunnel capacitors which consist of a metal droplet sandwiched between thick and thin oxide layers which, in turn, are sandwiched between metal electrodes. While tunneling of charge onto a metal droplet takes place in the tunnel capacitor arrangement, there is no passage of charge from a semiconductor to a metal particle disposed in a region of dielectric. Also, charge storage times in the tunnel capacitor regime are extremely short.

The present invention provides a memory device comprising a substrate of semiconductor material, an electrode disposed in overlying relationship with the substrate, an insulating material disposed between the substrate and the electrode, and a plurality of discrete noninteracting particles disposed in the insulating material at a distance from the surface of the substrate sufficient to permit tunneling between the particles and the semiconductor substrate, in which the particles are of a material capable of trapping electronic charge.

Semiconductor devices according to the present invention have the capability of retaining charge for a relatively long period of time after a signal which placed the charge in a desired condition is removed. One device according to the invention consists of an oxide layer such as silicon dioxide disposed on the surface of a semiconductor such as silicon and having a thickness sufficient to support tunneling. Particles of a metal such as platinum or silver or of a semiconductor are disposed on the surface of the silicon dioxide layer. A second layer

of silicon dioxide or silicon nitride, for example, is disposed in overlying relationship with the silicon dioxide layer and the particles. A metal electrode is provided on the second layer. The silicon dioxide thickness is approximately 30Å thereby permitting tunneling of charge carriers between the semiconductor and the discrete states of the plurality of small particles. The charge stored on the small particles causes a large, controllable hysteresis in the capacitance-voltage characteristic of the device which may be described in terms of an energy level model. The resulting device is particularly amenable for use as a memory element in arrangements which store digital data.

The semiconductor material can be N or P conductivity type and of a material selected from a group consisting of any known semiconductor element or compound taken from groups II, III, IV, V and VI of the Periodic Table of the Elements. The insulating material is specified as one selected from the group consisting oxides, nitrides, tellurides, chlorides, selenides and fluorides of the semiconductor material. Typical examples are thermally grown silicon dioxide and deposited silicon nitride. Deposited aluminium oxide or magnesium oxide may also be utilized.

The particles which are capable of trapping electronic charge are more specifically defined as being either semiconductor materials or metals. The metals are still more specifically characterized as refractory, or noble metals such as platinum or silver. The size of the particles are defined as being 100Å and below in size. The spacing between particles is required to be sufficient to prevent conduction of charge between the particles and a preferred distance is specifically defined as at least 30Å. The particles which are artificially generated substitutes for natural traps may consist of groups of ions which are implanted from an external ion source.

The insulating material disposed between the substrate and the electrode may be of a single insulating material, but in another embodiment, may consist of first and second layers of the same or different insulating material. In such embodiment, a layer thin enough to allow tunneling is deposited on the surface of the substrate. Particles are then formed by a fast vacuum deposition, for example, at high deposition rates on the surface of the first insulating layer. Subsequently, a thicker layer of insulation is formed in overlying relationship with the first layer and with the particles disposed on its surface. As indicated previously, the second insulating layer may be of a material which is the same as the first layer or it may be of different insulation from the first layer. The only criterion to be adhered to is that the insulating materials, when different, be compatible in the integrated circuits environment.

The invention will now be described by way of example, with reference to the drawings, in which:—

Figure 1 is a cross-section of the memory device according to the present invention showing a plurality of discrete, noninteracting particles which are capable of trapping electronic charge disposed in an insulating medium which is sandwiched between a semiconductor and a metal gate electrode;

Figure 2 shows the capacitance (normalized to the oxide capacitance) as a function of applied voltage on the metallic gate electrode of the device shown in Figure 1, taken on samples with and without small metal particles disposed between insulating films in an n-type silicon-silicon dioxide-aluminium oxide-silver structure. The solid line curve shows data obtained with particles present while the dashed line curve was obtained without particles; and

Figures 3A to 3F show a proposed energy level model which describes the effect of small particles which are capable of trapping electronic charge which tunnels from the semiconductor material to the small metal particles which properly are disposed between the semiconductor and a gate electrode.

Figure 1 shows a cross-section of a memory element or device according to the present invention. Substrate 1 is formed from a chip of semiconductor material which may be any known semiconductor element or compound taken from groups II, III, IV, V and VI of the Periodic Table of the Elements. A typical semiconductor material is silicon and a typical compound is gallium arsenide. In the description that follows, while it is appreciated that any semiconductor material may be utilized, silicon will be utilized as the preferred semiconductive material. Substrate 1 requires little processing other than that usually required in device manufacture and may be purchased in wafer form from commercial sources. Silicon has been chosen as the preferred embodiment because it has a relatively large band gap making it amenable to room temperature operation. Where the semiconductor materials have relatively small bandgap, temperatures which are lower than room temperature may be required and in some instances cryogenic temperatures may be required.

Using a preferred fabrication technique, after initial processing, a layer 2 of silicon dioxide is thermally grown on a surface of semiconductor substrate 1. Layer 2 may be formed by heating in steam or oxygen at a temperature of 850°C or may be deposited by vacuum deposition, sputtering or other

technique well known to those skilled in the semiconductor art.

The thermal growth or deposition of layer 2 should be carried out for a time sufficient to provide a thickness sufficient to support tunneling. Layer 2 is therefore grown or deposited to a thickness of approximately 30Å. In addition to the thermal oxides, thin insulators of phosphosilicate glass, aluminum or magnesium oxide may be utilized. Further, nitrides, tellurides, chlorides, selenides and fluorides of silicon may be utilized instead of the thermally grown silicon dioxide layer.

In Fig. 1 a plurality of discrete non-interacting particles 3 is shown disposed on the surface 4 of silicon dioxide layer 2. Particles 3 which must be capable of trapping charge may be formed from semiconducting or metallic materials. The refractory metals such as molybdenum and noble metals such as platinum and silver may be utilized in the practice of the present invention. In the embodiment of Fig. 1, particles 3 of platinum or silver are deposited on oxide layer 2 by rapid thermal evaporation to obtain particles 3 having sizes of about 30Å which are discrete and non-interacting with one another as far as charge conduction is concerned. A six second deposition of platinum or silver from a heated crucible in a vacuum chamber at a rate of 5Å/sec. provides the desired particle size. While a distribution in the size of the nuclei is generally encountered, nominal particle size is easily controlled by keeping either the evaporation time or evaporation rate small. The deposition of particles 3 is carried out in standard vacuum apparatus well known to those skilled in the semiconductor art.

After deposition of particles 3, insulating layer 5 which is thick compared to insulating layer 2 is then deposited over particles 3 and the exposed portions of surface 4 of layer 2. Layer 5 has a thickness of approximately 750Å and may consist of the same insulating material as layer 2 or may be a different insulating material from that used for insulating layer 2. Thus, where the insulating layers are of the same material, pyrolytic SiO_2 may be deposited on layer 2 and, where the layers are of different materials, sputtered or pyrolytic Si_3N_4 may be deposited on layer 2. Decomposition of silane in oxygen may be used to provide the desired oxide layer 5. In the embodiment of Fig. 1, layer 5 is formed of thermally evaporated aluminum oxide obtained from a heated crucible of aluminum oxide in a vacuum chamber. In general, insulating layer 5 may be any insulating material provided it is relatively pinhole free and possesses a relatively high breakdown voltage. Thus, material such as ceramics and plastics would be acceptable provided all other criteria of the integrated circuit environment are satisfied.

In Fig. 1, top or gate electrode 6 is shown disposed atop insulating layer 5. Electrode 6 may be compatible with the integrated circuits environment. The metal for electrode 6 may be provided by evaporation, vacuum deposition or sputtering, using well known techniques in such a way that the entire surface of layer 5 is covered with the metal. Utilizing well known photolithographic masking and etching techniques, electrode 6 is delineated and formed to have any desired configuration.

In a similar manner, an ohmic bottom electrode 7 is provided on the lower surface of semiconductor substrate 1. Again using well known photolithographic masking and etching techniques, a region of conductive material such as an alloy of indium-gold is delineated and formed on the surface of semiconductor substrate 1. By subjecting the wafer to an appropriate alloying temperature for the indium-gold alloy, ohmic contact 7 is formed on the bottom surface of substrate 1. Any suitable metal or alloy may be utilized as long as it forms an ohmic contact with the semiconductor substrate being utilized.

Until now, the device of Fig. 1 has been described as a two terminal device, but it should be appreciated that the two terminal device of Fig. 1 can be converted to a three terminal variable threshold voltage field effect transistor by the simple expedient of diffusing a pair of regions 8 of opposite conductivity type to substrate 1 into substrate 1. Regions 8 in substrate 1 act as source and drain of a field effect transistor, while electrode 6 acts as a gate. Region 8 may be formed after deposition of insulating layer 5 by opening suitable apertures in layers 2 and 5, and diffusing in dopants such as boron, arsenic or indium to provide the desired region of opposite conductivity type. By suitable masking, depositing and etching, the source and drain metallizations 9 may be deposited and delineated at the same time and may be of the same metal as electrode 6. Source and drain regions 8 need not be diffused but may be formed in accordance with well known Schottky barrier device techniques.

In the foregoing description of Fig. 1, the insulating medium on the surface of substrate 1 has been shown consisting of a thin oxide layer 2 and a thicker insulating layer 5, the latter overlying both the oxide layer 2 and a plurality of particles 3 disposed on the surface of layer 2. Insulating layers 2 and 5 may be of the same or different insulating materials. Where the insulating layers are of the same material, layers 2 and 5 may be deposited as a single layer of desired thickness. Then, using an ion implantation ap-

paratus, metal or semiconductor ions may be implanted within the insulator to any desired depth. In the present instance, groups of ions are substituted for particles 3 and are spaced from the surface of semiconductor substrate 1 at a distance which will permit tunneling from the surface of layer 1 to the groups of ions. The groups of ions which are substituted for particles 3 should form discrete non-interacting groups which are capable of storing electronic charge and should be spaced from one another a distance which does not permit charge conduction between the groups. Using commercially available equipment, the groups of ions which are substituted for particles 3 can be implanted and spaced quite accurately by adjusting the accelerating voltage of the implantation apparatus and by electronically deflecting the ion beam. Suitable ions include indium and niobium.

Referring now to Fig. 2, there is shown therein capacitance data (normalized to the oxide capacitance) as a function of applied voltage on gate electrode 6. The data was taken on samples with and without small metal particles disposed at the interface of insulating layers 2 and 5 in a structure consisting of an n-type silicon substrate 1 having a resistivity of approximately two ohm-centimeters; a layer 2 of silicon dioxide; a layer 5 of aluminum oxide and an electrode 6 of silver. In Fig. 2, the solid line curve shows data obtained with particles 3 present at the interface between layers 2 and 5 while the dashed line curve was obtained without particles. The thickness of layers 2 and 5 was 25Å and 750Å, respectively. Where particles 3 were utilized, platinum was evaporated to form particles 3 at a nominal size of 35Å. A large hysteresis effect is observed in the device with particles 3 while a very small hysteresis effect is observed in the sample without particles 3. The arrows on both the solid and dashed line curves indicate the direction in which the loop is traversed. In Fig. 2, the hysteresis loop saturates at about −15 volts while for smaller bias swings narrower hysteresis loops (not shown) are obtained. In general, it is possible to swing the flat band voltage to small positive values by biasing electrode 6 positively. It should be clear from Fig. 2 that the application of negative biases of approximately 15 volts can shift the capacitance characteristic (V_{fb}) by approximately 10 volts. This shift would then be reflected in a threshold voltage shift when the structure of Fig. 1 is used as a fielw effect transistor with electrode 6 acting as the gate of the field effect transistor. The hysteresis characteristic, as shown in Fig. 2, can be reproducibly retraced many times. The memory effect obtained, that is, the storage of electronic charge on particles 3 at the interface of insulating layers 2 and 5, appears to be a function of the quality of thin insulation layer 2. Thus, where the quality of insulating layer 2 is poor, a slow decay of the capacitance may be expected. However, where the quality of layer 2 is good, characteristics have been obtained which are stable for relatively long periods of time. In connection with the dashed line curve of Fig. 2, the small hysteresis effects observed are presumably due to unknown interface states that exist at the interface between insulation layers 2 and 5 and magnitude of hysteresis is too small to be of any practical use. It is, of course, obvious that where the hysteresis effect is large, that at least two stable, spaced and easily detectable storage states are achieved.

Referring now to Figs. 3A to 3F, there is shown therein a proposed energy level model which describes the effect of small particles which are capable of trapping electronic charge which tunnels from the semiconductor substrate 1 to the small metal particles 3 of the device of Fig. 1. For simplicity, the states of a metal particle 3 are represented by a ladder-like array of energy levels in a single insulator spaced within a tunneling distance of the surface of semiconductor substrate 1. For an additional discussion on the nature of these states, the following references may be reviewed:

"Charge-quantization Studies Using a Tunnel Capacitor", John Lamb and R. C. Jaklevic, *Physical Review Letters, 22,* 1371, (1969).

"Tunneling, Zero-Beam Anomalies, and Small Semiconductors", by H. R. Zeller and I. Giaver, *Physical Review, 181,* 789, (1969).

The separation of the energy levels in Fig. 3A is proportional to e^2C, where e is the electronic charge and C is equal to $\epsilon A/D$ with $A \sim l^2$ where l is a typical particle dimension. With $l = 35$Å and $D = 750$Å, e^2/C is greater than 0.1 eV. There also exists metal particle states for allowed discrete values of wave vector k to which electrons in the conduction band of the semiconductor can tunnel directly. However, the energy separation between these allowed k-values is significantly greater than that due to e^2/C. Thus, these terms have not been included in the model of Figs. 3A—3F. In addition, the discreteness of the proposed model is modified by the distribution in particle sizes. As modified by the foregoing, it may be seen that Fig. 3A illustrates a possible energy band scheme. In Fig. 3A, the energy level of the valence band is designated by E_v; the energy level of the conduction band is designated E_c and the Fermi level is designated E_f. In Fig. 3A, the states of a particle 3 of Fig. 1 are shown in an insulator 10 which is sandwiched between a semiconductor region 11 and a metallic region 12. A voltage is normally applied across region 12 to affect

the charge condition of a particle 4 which is disposed within insulating region 10. Occupied states of a particle 3 are shown in Fig. 3A as black dots and are also designated by the reference numbers 13 and 14. An unoccupied state of a particle 3 is shown in Fig. 3A by a circle and is also designated by reference number 15.

As a positive voltage V is applied, electrons in the conduction band can tunnel into the first unoccupied state 15 as shown in Fig. 3B converting unoccupied state 15 into occupied state 15^1 with an accompanying barrier change. The tunneling of an electron from the conduction band is shown by arrow 16 in Fig. 3B.

Reducing the voltage back toward zero causes flat bands with the applied bias still positive as shown in Fig. 3C. As the voltage is further reduced, electrons tunnel out of occupied state 15^1 converting it back to unoccupied state 15 and the semiconductor surface begins to be depleted of electrons causing the typical capacitance drop.

As the voltage is decreased negatively as shown in Fig. 3D, the next occupied level 14 loses its electron as shown by arrow 17 converting that state to an unoccupied state 14^1 and the surface of the semiconductor region 11 is still in a depleted condition. As the voltage is now increased back toward zero as shown in Fig. 3E, flat bands are achieved with the applied bias still negative and the capacitance increases to C_o. With a further decrease in the applied voltage to zero, the stable configuration to Fig. 3F is obtained. Thus, the flat band voltage and the corresponding capacitance change can be shifted from positive to negative bias. It should be appreciated that if, initially, band bending in the semiconductor 11 is encountered (e.g., due to charged impurities in the insulators), the hysteresis loop will be shifted, as was the case for the sample shown in Figure 2. An important point to be observed in Figure 3F is that the unoccupied level 14^1 of a particle 3 is opposite the unoccupied energy gap of the semiconductor 11 and thus can only only be populated by a less probable indirect tunneling process involving a thermally excited electron.

As a check on the above model, the change in the stored charge per cm^2, Q_s, can be computed from the area under the solid line hysteresis loop of Figure 2. This computation gave a value of Q_s approximately equal to 1.5×10^{12} electrons per cm^2. Assuming a uniform density of noninteracting particles 3 with a 50Å cell size under electrode 6, gives an average of approximately 1.5 electrons transferred per particle in going around the hysteresis loop. This resulted in good agreement with the proposed model shown in Figures 3A—3F.

While the device of Figure 1 has been discussed principally as a voltage variable capacitor having storage capability, it should be appreciated that the field effect transistor mode is the preferred mode of operation for devices according to the present invention. The three terminal mode of operation of the device of Figure 1 has application in memory arrangements which presently utilize MNOS devices, e.g., variable threshold field effect transistors and other charge storage devices. As with the two terminal variable capacitance arrangement, the voltage swing required is substantially less than that required for conventional MNOS devices. A voltage swing of 15 volts or less is typical for devices of the present application while prior art MNOS devices require higher voltage swings.

WHAT WE CLAIM IS:—

1. A memory device comprising a substrate of semiconductor material, an electrode disposed in overlying relationship with the substrate, an insulating material disposed between the substrate and the electrode, and a plurality of discrete noninteracting particles disposed in the insulating material at a distance from the surface of the substrate sufficient to permit tunneling between the particles and the semiconductor substrate, in which the particles are of a material capable of trapping electronic charge.

2. A device as claimed in claim 1, including source and drain regions formed in the substrate and in which the electrode is a gate electrode.

3. A device as claimed in claim 2, including electrodes connected to the source and drain regions.

4. A device as claimed in any one of the preceding claims, in which the semiconductor material is any known semiconductor element or compound taken from Groups II, III, IV, V and VI of the Periodic Table of the Elements.

5. A device as claimed in any one of the preceding claims, in which the semiconductor material is doped to exhibit p- or n-type conductivity.

6. A device as claimed in any one of the preceding claims, in which the insulating material is a glass; or an oxide, a nitride, a telluride, a chloride, a selenide, or a fluoride of a semiconductor; or an oxide of a metal.

7. A device as claimed in any one of the preceding claims, in which the particles are of semiconductor and metals.

8. A device as claimed in claim 7, in which the particles are refractory or noble metals.

9. A device as claimed in claim 8, in which the particles are platinum or silver.

10. A device as claimed in any one of the preceding claims, in which the particles are 100Å or smaller in size.

11. A device as claimed in claim 10, in which the distance is at least 30Å.

12. A device as claimed in any one of claims 1 to 7, in which the particles consist of groups of ions implanted from an external ion source.

13. A device as claimed in any one of the preceding claims, in which the electrode is of a metallic material.

14. A device as claimed in claim 13, in which the metallic material is aluminium or silver.

15. A device as claimed in any one of the preceding claims, in which the insulating material comprises a first layer of insulation having a thickness sufficient to support tunneling disposed on the substrate, and a second layer of insulation disposed in overlying relationship with the particles and the first layer.

16. A device as claimed in claim 15, in which the first and second layers are of the same insulating material.

17. A device as claimed in claim 15, in which the first and second layers are of different insulating materials.

18. A memory device substantially as described with reference to Figure 1, 2 or 3 of the drawings.

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Agent for the Applicants.

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2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

FIG. 1

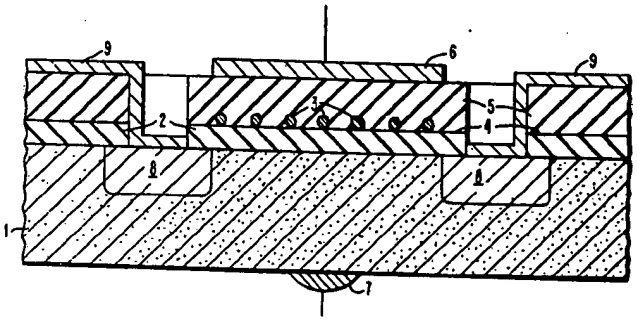

FIG. 2

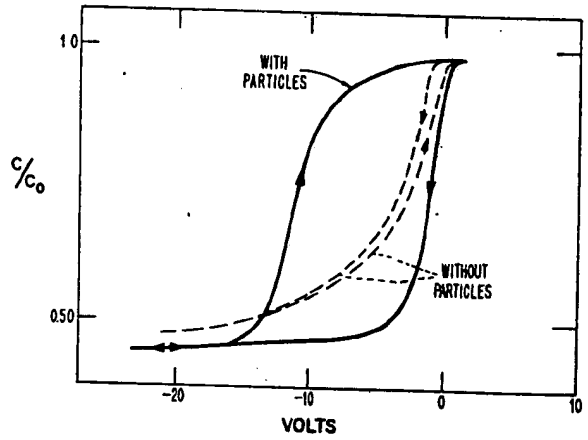

FIG. 3A

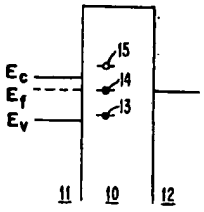

FIG. 3B

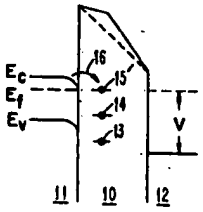

FIG. 3C

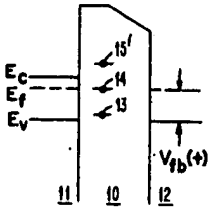

FIG. 3D

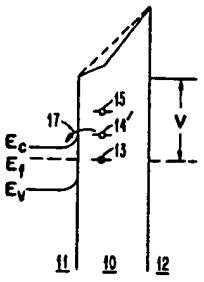

FIG. 3E

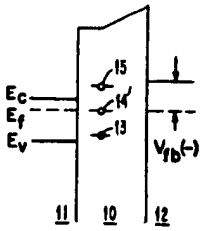

FIG. 3F